REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application are respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims are respectfully requested.

Status of Claims

Claims 1-9 and 14-18 are pending in the application.

The Telephone Interview

Initially, Applicants wish to thank the Examiner, William Wood, for granting and attending the telephone interview on May 17, 2006, with Applicants' Representatives.

In the Interview, Applicant's representatives asserted that claims 1, 6, 14 and 17 would be allowable over the cited references. Specifically, Applicant's representatives asserted that Osborne does not describe, teach or fairly suggest counting a number of noise events in which a direct-current offset value of a chip is bigger than a noise floor value; and/or updating the noise floor value based on the number of the noise events. More particularly, Applicant's representatives asserted that, in contrast to counting noise events, as recited by claims 1, 6, 14 and 17, the counter described by Osborne merely counts a pre-established duration of a calibration interval. The Examiner stated that a further review of the

cited references may be required before determining whether the pending claims would be allowable over the cited references.

CLAIM REJECTIONS

35 U.S.C. § 102 Rejections

In the Office Action, the Examiner rejected claims 1-9 and 14-16 under 35 U.S.C. § 102(b), as being anticipated by Osborne et al. (US 4,225,976). Specifically, the Examiner contended that Osborne et al. describes a noise floor register to store a noise floor value of a chip (element 1; column 1, line 53); a noise event counter to count a number of events in which a direct-current offset value of the chip is bigger than the noise floor value (column 2, lines 7-10; column 5, lines 4-7); and an approximator to update the noise floor register with an approximated noise floor value (column 1, lines 61-64) by performing the following operations one or more times: causing the noise event counter to count the noise events (column 1, lines 61-64); and updating the noise floor value based on the number of the noise events (column 5, lines 4-7; operation continues based upon a certain number of counts).

Applicants respectfully traverse this rejection of claims 1-9 and 14-16 in view of the remarks that follow.

As is well established, in order to successfully assert a prima facie case of anticipation, the Examiner must provide a single prior art document that teaches every element and limitation of the claim or claims being rejected.

As discussed in detail below, Applicants respectfully submit that Osborne et al. does not disclose, teach or fairly suggest one or more of the features recited by claims 1, 6, and 14.

Each of independent claims 1, 6, and 14 recite, in paraphrase, storing a noise floor value of a chip; determining an approximated noise floor value by performing the following operations one or more times: counting a number of noise events in which a direct-current offset value of a chip is bigger than said noise floor value; and updating said noise floor value based on the number of said noise events (emphasis added). It is respectfully asserted that Osborne et al. does not teach or fairly suggest at least this feature of the claimed invention, as discussed in detail below.

In the portions of the Osborne reference cited by the Examiner, Osborne et al. refers to a control counter (element 22 in the single Fig.) to control a duration of a calibration interval by counting clock pulses up to a prescribed number and to prevent further accumulation of noise reference values (column 2, lines 6-10; column 5, lines 4-9). The control counter described by Osborne et al. counts up to a prescribed number of clock pulses in order to measure a predefined time interval (column 2, lines 8-9). This counting is not relevant in any way to counting of noise events, as recited in claims 1, 6, and 14.

Applicants respectfully assert that, in contrast to the clock pulses counted by Osborne et al., the counting of noise events, as recited in claims 1, 6, and 14, relates to counting events in which a direct current offset value of a chip is bigger than the noise floor value. In addition, it will be appreciated that prior to counting the number of noise events, the number of the counted noise events may be unknown. Thus, in contrast to Osborne et al., which describes counting the predefined number of clock pulses, claims 1, 6, and 14 relate to counting a number of noise events, which is not predefined.

Furthermore, based on a careful review of the entire disclosure of Osborne et al., Applicants respectfully assert that there is no mention in the Osborne reference of performing any counting of a number of noise events.

Thus, it is respectfully requested that the rejection of independent claims 1, 6, and 14 under 35 U.S.C. 102§(b) in view of Osborne et al. be withdrawn.

Furthermore, it is respectfully submitted that independent claims 1, 6, and 14 are patentable, and thus allowable, over the prior art references on record and any combination thereof. In this regard, it is noted that the distinguishing features of independent claims 1, 6, and 14 as discussed above, would not have been obvious at the time the invention was made to a person skilled in the art, in view of Osborne et al., alone or in combination with any other cited references.

Claims 2-5 depend, directly or indirectly, from independent claim 1 and incorporate all the elements of this claim. Claims 7-9 depend, directly or indirectly, from independent claim 6 and incorporate all the elements of this claim. Claims 15-16 depend, directly or indirectly, from independent claim 14 and incorporate all the elements of this claim. Therefore, it is respectfully submitted that claims 2-5, 7-9, and 15-16 are patentable, and thus allowable, at least for the reasons set forth above.

35 U.S.C. § 103 Rejections

In the Office Action, the Examiner rejected claims 17 and 18 under 35 U.S.C. § 103(a), as being unpatentable over Osborne et al. (US 4,225,976) in view of Gupta et al. (US 6,766,176).

Applicants respectfully traverse this rejection of claims 17 and 18 in view of the remarks that follow.

As is well established, in order to establish a prima facie case of obviousness, the prior art references must teach or suggest all the claim limitations.

Independent claim 17 recites, in paraphrase, storing a noise floor value of a chip; determining an approximated noise floor value by performing the following operations one or more times: counting a number of noise events in which a direct-current offset value of a chip is bigger than said noise floor value; and updating said noise floor value based on the number of said noise events.

It is respectfully asserted that Osborne et al. does not teach or fairly suggest at least this feature of the claimed invention, as discussed in detail above with reference to claims 1, 6, and 14. This deficiency of Osborne is not cured by Gupta et al., which also does not teach or fairly suggest at least this feature of the claimed invention. Therefore, a prima facie case of obviousness cannot be established with regard to claim 17.

Accordingly, it is respectfully requested that the rejection of claim 17 under 35 U.S.C. §103(a) be withdrawn.

Claim 18 depends directly from independent claim 17 and incorporates all the elements of this claim. Therefore, it is respectfully submitted that claim 18 is patentable, and thus allowable, at least for the reasons set forth above.

In view of the foregoing amendments and remarks, the pending claims are deemed to be allowable. Their favorable reconsideration and allowance are respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 50-3355.

Respectfully submitted,

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